WHAT IS CLAIMED IS:

1. A high density semiconductor structure having a plurality of integrated circuit chips, comprising:

a first integrated circuit chip having an upper bonding surface;

a second integrated circuit chip secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip;

a chip insulating layer disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the enclosed regions of air causes the dielectric constant of the chip insulating layer to be less than the dielectric constant of the insulating material.

2. The semiconductor structure of Claim 1 further comprises a conductor insulating layer formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein the enclosed regions of air causes the dielectric constant of the conductor insulating layer to be lower than the dielectric constant of the insulating material.

3. The semiconductor structure of Claim 1 wherein the chip insulating layer comprises a foamed polymeric material.

4. The semiconductor structure of Claim 2 wherein the conductor insulating layer comprises a foamed polymeric material.

5. The semiconductor structure of Claim 3 wherein the foamed polymeric material comprises a foamed polyimide.

6. The semiconductor structure of Claim 5 wherein the foamed polyimide is approximately 2.1 microns thick.

7. The semiconductor structure of Claim 3 wherein the foamed polymeric material comprises a hydrophobic material wherein the hydrophobic material is treated so as to provide the material with hydrophilic properties.

8. The semiconductor structure of Claim 7 wherein the foamed polymeric material comprises polynorbornene.

9. The semiconductor structure of Claim 1 wherein each enclosed region of air is less than 1 micron.

10. The semiconductor structure of Claim 1 wherein each enclosed region of air is approximately 0.1 micron.

11. The semiconductor structure of Claim 2 wherein each enclosed region of air is less than the minimum distance separating adjacent conductive leads.

12. The semiconductor structure of Claim 1 wherein the dielectric constant of the chip insulating layer is approximately one third of the dielectric constant of the insulating material.

13. The semiconductor structure of Claim 12 wherein the dielectric constant of the insulating layer is less than 1.5.

14. The semiconductor structure of Claim 1 wherein the conductive leads are made of an aluminum alloy.

15. The semiconductor structure of Claim 1 further comprises a third integrated circuit chip wherein the third chip is secured to the second chip in a manner such that a lower surface of the third chip is positioned adjacent an upper surface of the second chip wherein a third insulating layer is disposed between the second and third chips.

16. The semiconductor structure of Claim 15 wherein the third insulating layer comprises a foamed polymeric material.

17. The multichip cube structure of Claim 16 wherein the first integrated circuit chip further comprises a lower surface wherein a fourth insulating layer is formed on the lower surface of the first chip.

18. The multichip cube structure of Claim 17 wherein the fourth insulating layer comprises a foamed polymeric material.

19. A multichip cube structure having a plurality of integrated circuit chips, comprising:

a first integrated circuit chip having a first insulating layer disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant, wherein at least a portion of the first insulating layer contains enclosed regions of air that reduce the dielectric constant of the first insulating layer to a value lower than the first dielectric constant;

a second integrated circuit chip secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;

a second insulating layer disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant, wherein at least a portion of the second insulating layer contains a plurality of enclosed regions of air that reduce the dielectric constant of the second insulating layer to a value lower than the first dielectric constant.

20. The multichip cube structure of Claim 19 wherein the first insulation material comprises a polymeric material.

21. The multichip cube structure of Claim 20 wherein the polymeric material is treated with a supercritical fluid so as to produce the enclosed regions of the air in the material.

22. The multichip cube structure of Claim 19 wherein each enclosed region of air is less than the distance between adjacent metal leads on the upper surface of the first chip.

23. The multichip cube structure of Claim 19 wherein the second insulating material comprises a polymeric material.

24. The multichip cube structure of Claim 23 wherein the polymeric material is polyimide.

25. The multichip cube structure of Claim 20 wherein the polymeric material is polynorbornene.

26. The multichip cube structure of Claim 25 wherein the insulating material is treated with a hydrogen containing radical so as to make the surface more hydrophilic.

27. A method of manufacturing a multichip cube structure having reduced capacitive loading, comprising:

forming an insulating layer on an upper bonding surface of a first chip;

reducing the dielectric constant of the insulating layer by creating a plurality of voids in the insulating layer;

securing a second chip to the upper bonding surface of the first chip wherein a lower bonding surface of the second chip is positioned adjacent the upper bonding surface of the first chip.

28. The method of Claim 27 wherein creating a plurality of voids in the insulating layer comprises exposing the insulating layer to a supercritical fluid.

29. The method of Claim 28 wherein exposing the insulating layer to the supercritical fluid comprises exposing the insulating layer to carbon dioxide.

30. The method of Claim 27 wherein securing the second chip to the upper bonding surface of the first chip comprises using an adhesive.

31. The method of Claim 27 wherein forming the insulating layer on the upper bonding surface of the first chip comprises forming an insulating layer having embedded adhesives.

32. The method of Claim 27 wherein forming the insulating layer comprises forming a polyimide layer.